# Master Thesis

## Integration of a Real-time Coherent FPGA-Based Communication Link with Ethernet Transmit and Receive Data

Karlsruhe Institute of Technology

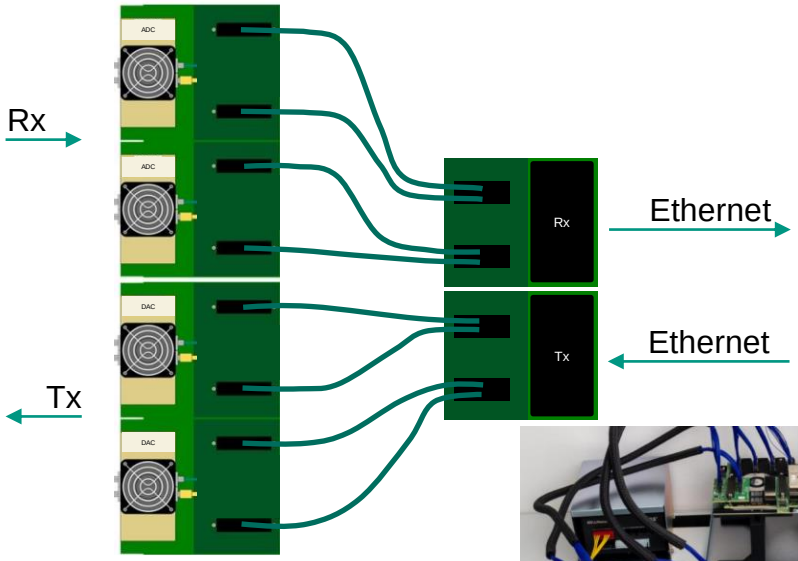
Over the past few years, the demand for higher data rate wireless communications for personal and industrial applications has increased. To meet this demand, the upcoming 6th generation standard considers frequencies in the range of 250-320GHz to provide bandwidth up to 70GHz. The vision is to achieve data rates of up to 250 Gbit/s per direction and polarization. To enable the generation and processing of data, Field Programmable Gate Arrays (FPGAs) play an important role. In the framework of a coherent communication system, two Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) are employed. Realizing real-time signal processing necessitates the transmission and reception of signals to and from a single processing FPGA through high-speed synchronous transfer.

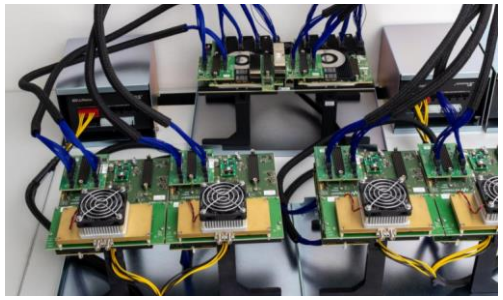
**Tasks:**

- Research on Ethernet, FPGA/VHDL and AXI stream.
- Setup and evaluation of coherent system in electric back-to-back configuration with two DACs and ADCs.
- Implementation of real-time processing of Tx and Rx data from/to a Ethernet interface.
- Evaluation of scalability to a two polarization coherent system with four DACs and ADCs.

**Requirements:**

- Experience in Python, VHDL/Verilog (basic).
- Knowledge in coherent communications.



**Interested? For more information contact:**

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