Master Thesis:

Real-time implementation of a carrier recovery scheme for a digital coherent optical receiver

Karlsruhe Institute of Technology

Coherent optical detection along with digital signal processing (DSP) enables mitigating various transmission impairments easily and adaptively [1]. Though, the first step of the DSP development is often based on the use of high speed sampling oscilloscopes and software processing of stored data, true verification is only possible with real-time demonstration using hardware implementation. In research environments, field-programmable gate arrays (FPGAs) are often used for real-time implementation of DSP algorithms [2]. As the state-of-the- art FPGA can only operate at about a few hundred megahertz, therefore, the related DSP algorithms should be realized with a parallel structure rather than serial one. In such a case, it is very critical to design low-complexity DSP algorithms or simplify DSP algorithms in order to implement the real-time systems in a hardware- and power-efficient way. The goal of this thesis is to implement a carrier recovery (Frequency and phase estimation) scheme in FPGA.

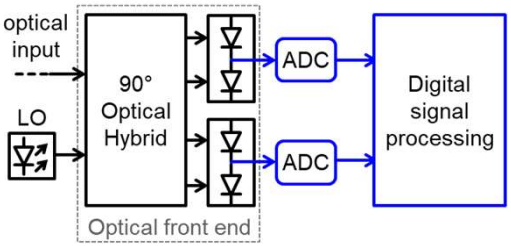

Fig. 1 An outline of a coherent optical receiver.

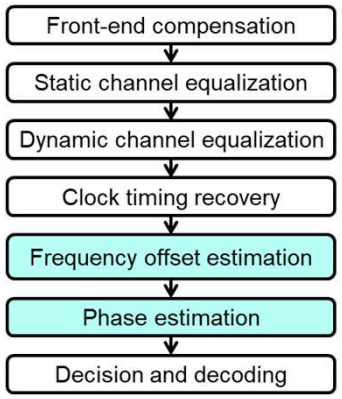

Fig. 2 Various signal processing steps

Your Tasks:

- Design and realization of DSP algorithms using hardware description language such as VHDL.
- Hardware implementation using Xilinx FPGA chip.
- Experiment using optical setup to benchmark the hardware performance with respect to offline DSP.

References:
[1] S. Savory, IEEE J. Sel. Topics Quantum Electron, 16, 5, (2010)
[2] Andreas Leven *et. al.,* IEEE J. Sel. Topics Quantum Electron, 16, 5, (2010)

For more information contact:

Salek Mahmud, M. Sc.
md.mahmud@kit.edu
Tel. 0721-608-47173

Prof. Dr. Sebastian Randel
sebastian.randel@kit.edu
Tel. 0721-608-42490